Remarks

The Office Action mailed November 12, 2004 has been carefully reviewed and the following remarks have been made in consequence thereof.

Claims 1-6 and 8-28 are now pending in this application. Claims 1-6, 11, 13-16, 20, and 22-25 are rejected. Claims 7-10, 12, 17-19, 21, and 26-28 are objected to. Claim 7 is canceled without prejudice, waiver, or disclaimer. Claims 1, 3, 8, 13, and 22 have been amended. No new matter has been added.

In accordance with 37 C.F.R. 1.136(a), a three-month extension of time is submitted herewith to extend the due date of the response to the Office Action dated November 12, 2004 for the above-identified patent application from February 12, 2005 through and including May 12, 2005. In accordance with 37 C.F.R. 1.17(a)(3), authorization to charge a deposit account in the amount of $1020.00 to cover this extension of time request also is submitted herewith.

Applicants respectfully traverse the statement in the Office Action that the Applicants have not given a post office address anywhere in the application papers as required by 37 C.F.R. §1.33(a). 37 C.F.R. §1.33(a) states, "When filing an application, a correspondence address must be set forth...in a clearly identifiable manner, in any paper submitted with an application filing." Applicants respectfully submit that a correspondence address was provided in a clearly identifiable manner in a Utility Patent Application Transmittal that was submitted with the present patent application. The Utility Patent Application Transmittal includes a heading "CORRESPONDING ADDRESS", which is clearly identifiable. A copy of the Utility Patent Application Transmittal is attached.

The rejection of Claims 3, 13, and 22 under 35 U.S.C §112, second paragraph, is respectfully traversed. Applicants have amended 3, 13, and 22 and respectfully submit that Claims 3, 13, and 22 particularly point out and distinctly claim the subject matter which the Applicants regard as their invention. Accordingly, Applicants respectfully request that the section 112 rejection to Claims 3, 13, and 22 be withdrawn.

The rejection of Claims 1-2 and 4-6 under 35 U.S.C. § 103(a) as being unpatentable over Danstrom (U.S. Patent No. 5,617,014) and Heaston, Jr. et al. (U.S. Patent 5,748,422), in view of Huang et al. (U.S. Patent 6,133,757) is respectfully traversed.

Claim 1 has been amended to include the recitations of Claim 7, which is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. For the reasons set forth above, Claim 1 is submitted to be patentable over Danstrom and Heaston, Jr. et al., in view of Huang et al.

Claims 2 and 4-6 depend directly from independent Claim 1. When the recitations of Claims 2 and 4-6 are considered in combination with the recitations of Claim 1, Applicants submit that dependent Claims 2 and 4-6 likewise are patentable over Danstrom and Heaston, Jr. et al., in view of Huang et al.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 1, 2, and 4-6 be withdrawn.

The rejection of Claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Kitamura (U.S. Patent No. 4,774,450), in view of Heaston, Jr. et al. is respectfully traversed.

Kitamura describes a comparator (40) having an output connected to a control input of an analog switch (42) inserted between an output terminal (20) and a resistor (24) (column 4, lines 59-62). Further, the output of the comparator is connected to control inputs of analog switches (44 and 46) associated with an error signal generator (12) and a drive circuit (14) (column 4, lines 62-65). The drive circuit is located within a power-supply circuit (column 4, lines 35-40).

Heaston, Jr. et al. describe a field effect transistor (FET) (14) that is a MOSFET and a transistor (32) that is a bipolar transistor (column 6, lines 34-39). The FET could be replaced by any similar semiconductor device, such as a bipolar power transistor, while the bipolar transistor could be replaced by a FET (column 6, lines 34-39).

Claim 11 recites a circuit for reducing thermal dissipation in a single PLC package, the circuit comprising "a drive circuit comprising a field effect transistor (FET) including a drain and a gate, said drive circuit located within a current regulator of a programmable logic controller; an output circuit including a load terminal, said output circuit connected to said drain; a feedback amplifier connected to said output circuit; and an error amplifier circuit connected to said feedback amplifier and to said gate."

Neither Kitamura nor Heaston, Jr. et al., considered alone or in combination, describe or suggest a circuit for reducing thermal dissipation in a single PLC package as recited in Claim 11. Specifically, neither Kitamura nor Heaston, Jr. et al., considered alone or in combination, describe or suggest a drive circuit including a field effect transistor (FET) including a drain and a gate, the drive circuit located within a current regulator of a programmable logic controller, an output circuit including a load terminal, the output circuit connected to the drain, and an error amplifier circuit connected to the feedback amplifier and to the gate. Rather, Kitamura describes a drive circuit associated with an analog switch that is connected to an output of a comparator. The drive circuit in Kitamura is located within a power-supply circuit. Heaston, Jr. et al. describe a field effect transistor. Accordingly, neither Kitamura nor Heaston, Jr. et al., considered alone or in combination, describe or suggest a drive circuit including a field effect transistor including a drain and a gate, where the drive circuit is located within a current regulator of a programmable logic controller. For the reasons set forth above, Claim 11 is submitted to be patentable over Kitamura in view of Heaston, Jr. et al.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claim 11 be withdrawn.

The rejection of Claims 14-16 under 35 U.S.C. § 103(a) as being unpatentable over Kitamura and Heaston, Jr. et al., in view of Huang et al. (U.S. Patent 6,133,757) is respectfully traversed.

Kitamura and Heaston, Jr. et al. are described above.

Huang et al. describe a method for manufacturing semiconductor circuits in which a switch speed of each NMOS FET is directly proportional to a driving current thereof (column 7, lines 47-49). That is, the more powerful the driving capability is, the faster the switch speed will be (column 7, lines 49-50).

Claims 14-16 depend directly from independent Claim 11 which recites a circuit for reducing thermal dissipation in a single PLC package, the circuit comprising "a drive circuit comprising a field effect transistor (FET) including a drain and a gate, said drive circuit located within a current regulator of a programmable logic controller; an output circuit including a load terminal, said output circuit connected to said drain; a feedback amplifier connected to said output circuit; and an error amplifier circuit connected to said feedback amplifier and to said gate."

None of Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a circuit for reducing thermal dissipation in a single PLC package as recited in Claim 11. Specifically, none of Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a drive circuit including a field effect transistor (FET) including a drain and a gate, the drive circuit located within a current regulator of a programmable logic controller, an output circuit including a load terminal, the output circuit connected to the drain, and an error amplifier circuit connected to the feedback amplifier and to the gate. Rather, Kitamura describes a drive circuit associated with an analog switch that is connected to an output of a comparator. The drive circuit in Kitamura is located within a power-supply circuit. Heaston, Jr. et al. describe a field effect transistor. Huang et al. describe an NMOS FET whose switch speed is directly proportional to a driving current. Accordingly, none of Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a drive circuit including a field effect transistor including a drain and a gate, where the drive circuit is located within a current regulator of a programmable logic controller. For the reasons set forth above, Claim 11 is submitted to be patentable over Kitamura and Heaston, Jr. et al., in view of Huang et al.

When the recitations of Claims 14-16 are considered in combination with the recitations of Claim 11, Applicants submit that dependent Claims 14-16 likewise are patentable over Kitamura and Heaston, Jr. et al., in view of Huang et al.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 14-16 be withdrawn.

The rejection of Claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Shamouilian et al. (U.S. Patent 6,432,282), in view of Kitamura, and Heaston, Jr. et al. is respectfully traversed.

Shamouilian et al. describe an individual conductor with a feedback portion (242) that connects each contact (56) individually to a controller (204) (column 4, lines 18-20). Each individual conductor with the feedback portion senses an electric current being applied to its particular contact (56), and provides input to the controller indicative of the electric current (column 20, lines 20-24). The controller relies upon this sensed electrical current to balance the electric current between the different contacts (56) (column 4, lines 24-26).

Kitamura and Heaston, Jr. et al. are described above.

Claim 20 recites a PLC comprising "a CPU; a bus interface operationally coupled to said CPU; at least one memory unit operationally coupled to said bus interface; at least one I/O module operationally coupled to said bus interface; and a current regulator operationally coupled to said I/O module, said current regulator comprising: a drive circuit comprising a field effect transistor (FET) including a drain and a gate, said drive circuit implemented as a pulse-width modulation circuit; an output circuit including a load terminal, said output circuit connected to said drain; a feedback amplifier connected to said output circuit; and an error amplifier circuit connected to said feedback amplifier and to said gate."

None of Shamouilian et al., Kitamura, and Heaston, Jr. et al., considered alone or in combination, describe or suggest a PLC as recited in Claim 20. Specifically, none of Shamouilian et al., Kitamura, and Heaston, Jr. et al., considered alone or in combination, describe or suggest a PLC including a current regulator operationally coupled to the I/O module, the current regulator including a drive circuit including a field effect transistor (FET) including a drain and a gate, the drive circuit implemented as a pulse-width modulation circuit, an output circuit including a load terminal, the output circuit connected to the drain, and an error amplifier circuit

connected to the feedback amplifier and to the gate. Rather, Shamouilian et al. describe an individual conductor with a feedback portion. The conductor senses an electric current being applied to its particular contact, and provides input to a controller indicative of the electric current. Kitamura describes a drive circuit associated with an analog switch that is connected to an output of a comparator. The drive circuit in Kitamura is located within a power-supply circuit. Heaston, Jr. et al. describe a field effect transistor. Accordingly, none of Shamouilian et al., Kitamura, and Heaston, Jr. et al., considered alone or in combination, describe or suggest a PLC including a current regulator operationally coupled to the I/O module, the current regulator including a drive circuit including a field effect transistor (FET) including a drain and a gate, where the drive circuit is implemented as a pulse-width modulation circuit. For the reasons set forth above, Claim 20 is submitted to be patentable over Shamouilian et al. in view of Kitamura, and Heaston, Jr. et al.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claim 20 withdrawn.

The rejection of Claims 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Shamouilian et al., Kitamura, Heaston, Jr. et al., in view of Huang et al., is respectfully traversed.

Shamouilian et al., Kitamura, Heaston, Jr. et al., and Huang et al. are described above.

Claims 23-25 depend directly from independent Claim 20 which recites a PLC comprising "a CPU; a bus interface operationally coupled to said CPU; at least one memory unit operationally coupled to said bus interface; at least one I/O module operationally coupled to said bus interface; and a current regulator operationally coupled to said I/O module, said current regulator comprising: a drive circuit comprising a field effect transistor (FET) including a drain and a gate, said drive circuit implemented as a pulse-width modulation circuit; an output circuit including a load terminal, said output circuit connected to said drain; a feedback amplifier connected to said output circuit; and an error amplifier circuit connected to said feedback amplifier and to said gate."

None of Shamouilian et al., Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a PLC as recited in Claim 20. Specifically, none of Shamouilian et al., Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a PLC including a current regulator operationally coupled to the I/O module, the current regulator including a drive circuit including a field effect transistor (FET) including a drain and a gate, the drive circuit implemented as a pulse-width modulation circuit, an output circuit including a load terminal, the output circuit connected to the drain, and an error amplifier circuit connected to the feedback amplifier and to the gate. Rather, Shamouilian et al. describe an individual conductor with a feedback portion. The conductor senses an electric current being applied to its particular contact, and provides input to a controller indicative of the electric current. Kitamura describes a drive circuit associated with an analog switch that is connected to an output of a comparator. The drive circuit in Kitamura is located within a power-supply circuit. Heaston, Jr. et al. describe a field effect transistor. Huang et al. describe an NMOS FET whose switch speed is directly proportional to a driving current. Accordingly, none of Shamouilian et al., Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest a PLC including a current regulator operationally coupled to the I/O module, the current regulator including a drive circuit including a field effect transistor (FET) including a drain and a gate, where the drive circuit is implemented as a pulse-width modulation circuit. For the reasons set forth above, Claim 20 is submitted to be patentable over Shamouilian et al., Kitamura, Heaston, Jr. et al., in view of Huang et al.

When the recitations of Claims 23-25 are considered in combination with the recitations of Claim 20, Applicants submit that dependent Claims 23-25 likewise are patentable over Shamouilian et al., Kitamura, Heaston, Jr. et al., in view of Huang et al.

For at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 23-25 be withdrawn.

Moreover, Applicants respectfully submit that the Section 103 rejections of Claims 11, 14-16, 20, and 23-25 are not proper rejections. As is well established, obviousness cannot be established by combining the teachings of the cited art to

produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination. None of Shamouilian et al., Kitamura, Heaston, Jr. et al., and Huang et al., considered alone or in combination, describe or suggest the claimed combination. Furthermore, in contrast to the assertion within the Office Action, Applicants respectfully submit that it would not be obvious to one skilled in the art to combine Shamouilian et al. with Kitamura, Heaston, Jr. et al., or Huang et al., because there is no motivation to combine the references suggested in the cited art itself.

As the Federal Circuit has recognized, obviousness is not established merely by combining references having different individual elements of pending claims. Ex parte Levengood, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993). MPEP 2143.01. Rather, there must be some suggestion, outside of Applicants' disclosure, in the prior art to combine such references, and a reasonable expectation of success must be both found in the prior art, and not based on Applicants' disclosure. In re Vaeck, 20 U.S.P.Q.2d 1436 (Fed. Cir. 1991). In the present case, neither a suggestion or motivation to combine the prior art disclosures, nor any reasonable expectation of success has been shown.

Furthermore, it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the cited art so that the claimed invention is rendered obvious. Specifically, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the art to deprecate the claimed invention. Further, it is impermissible to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. The present Section 103 rejections are based on a combination of teachings selected from multiple patents in an attempt to arrive at the claimed invention. Specifically, Shamouilian et al. teach an individual conductor with a feedback portion. The conductor senses an electric current being applied to its particular contact, and provides input to a controller indicative of the electric current. Kitamura teaches a drive circuit associated with an analog switch that is connected to an output of a comparator. The drive circuit in Kitamura is located within a power-supply circuit. Heaston, Jr. et al. teach a field effect transistor. Huang et al. teach an NMOS FET whose switch speed is directly proportional to a driving current. Since

there is no teaching nor suggestion in the cited art for the combination, the Section 103 rejections appear to be based on a hindsight reconstruction in which isolated disclosures have been picked and chosen in an attempt to deprecate the present invention. Of course, such a combination is impermissible, and for this reason alone, Applicants request that the Section 103 rejections of Claims 11, 14-16, 20, and 23-25 be withdrawn.

For at least the reasons set forth above, Applicants respectfully request that the rejections of Claims 11, 14-16, 20, and 23-25 under 35 U.S.C. 103(a) be withdrawn.

Claims 7-10, 12, 17-19, 21, and 26-28 have been indicated to contain allowable subject matter if rewritten to include all of the limitations of the respective base claims and any respective intervening claims.

Claim 7 has been canceled.

Claim 8 has been amended to include all the recitations of the base Claim 1. Accordingly, Claim 8 is in condition for allowance.

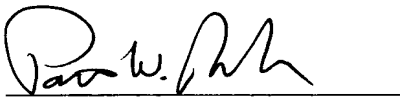
Claim 9 depends directly from independent Claim 8. For the reasons set forth above, Claim 9 is in condition for allowance.

Claim 10 depends from independent Claim 1, which is amended to include the recitations of Claim 7 indicated as allowable. Accordingly, Claim 10 is in condition for allowance.

Applicants thank the Examiner for the indication of allowable subject matter in Claims 12, 17-19, 21, and 26-28.

In view of the foregoing amendment and remarks, all the claims now active in this application are believed to be in condition for allowance. Reconsideration and favorable action is respectfully solicited.

Respectfully Submitted,



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